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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte JAMES L. TUCKER, GARY ROOSEVELT, KENNETH H. HEFFNER, and JAMES HOBBS

Appeal 2015-007529
Application 13/416,404
Technology Center 2800

Before TERRY J. OWENS, JEFFREY R. SNAY, and JENNIFER R. GUPTA, *Administrative Patent Judges*.

OWENS, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF THE CASE

The Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1, 2, 4–9, 11 and 21–25. We have jurisdiction under 35 U.S.C. § 6(b).

The Invention

The Appellants claim a vertically stacked integrated circuit layer system. Claim 1 is illustrative:

> 1. A system comprising:
> a first integrated circuit layer comprising a first plurality of interconnect elements;
> a second integrated circuit layer comprising a second plurality of interconnect elements, wherein the second

integrated circuit layer is a semiconductor device that comprises the second plurality of interconnect elements; and

a third integrated circuit layer positioned between the first and second integrated circuit layers, wherein the first, second, and third integrated circuit layers are stacked in a z-axis direction, and wherein the third integrated circuit layer comprises:

an interposer portion comprising an electrically conductive through-via, wherein the electrically conductive through-via is configured to communicate with at least one interconnect element of the first plurality of interconnect elements and at least one interconnect element of the second plurality of interconnect elements, and

an integrated circuit die adjacent to the interposer portion and between the first and second integrated circuit layers, wherein a surface of the integrated circuit die comprises an electrical contact electrically connected to the second integrated circuit layer, wherein the electrically conductive through-via of the interposer portion electrically connects the integrated circuit die with the first integrated circuit layer.

The References

Hayden	US 5,579,207	Nov. 26, 1996
Heffner	US 6,319,740 B1	Nov. 20, 2001
Tucker	US 2008/0129501 A1	June 5, 2008
Michaels	US 7,709,943 B2	May 4, 2010
Lin	US 8,183,087 B2	May 22, 2012 (filed Sep. 9, 2008)
Wang	US 8,716,873 B2	May 6, 2014 (filed July 1, 2011)

The Rejections

The claims stand rejected as follows: claims 1, 2, 9, 21, 22 and 24 under 35 U.S.C. § 102(b) over Hayden, claims 4–6 under 35 U.S.C. § 103 over Hayden in view of Tucker, claim 7 under 35 U.S.C. § 103 over Hayden in view of Heffner, claim 8 under 35 U.S.C. § 103 over Hayden in view of

Michaels, claim 11 under 35 U.S.C. § 103 over Hayden, claim 23 under 35 U.S.C. § 103 over Hayden in view of Lin and claim 25 under 35 U.S.C. § 103 over Hayden in view of Wang.

OPINION

The rejections are affirmed as to claims 1, 2, 4–9 and 21–23 and reversed as to claims 11, 24 and 25.

Claims 1, 2, 4–9 and 21–23

The Appellants argue claims 1, 2, 4–9 and 21–23 in the following groups: 1) claims 1, 7–9 and 21–23, 2) claim 2, and 3) claims 4–6 (App. Br. 6–20). Although the Appellants address claims 7, 8, and 21–23 under separate headings, the Appellants do not provide a substantive argument as to the separate patentability of those claims (App. Br. 11–19).[1] We therefore limit our discussion to claim 2 and one claim in each of the other groups, i.e., claim 1, which is the sole independent claim, and claim 4. Claims 7–9 and 21–23 stand or fall with claim 1, and claims 5 and 6 stand or fall with claim 4. *See* 37 C.F.R. § 41.37(c)(1)(iv) (2012).

Claim 1

Hayden discloses a system comprising a first integrated circuit layer (130) comprising a first plurality of interconnect elements (24, 26, 28, 30, 32, 34, 58), a second integrated circuit layer (10) comprising a second plurality of interconnect elements (24, 26, 28, 30, 32, 34, 58) and an integrated circuit chip (12), and a third integrated circuit layer (120) between

[1] *See In re Lovin*, 652 F.3d 1349, 1357 (Fed. Cir. 2011) (Rule 41.37 "require[s] more substantive arguments in an appeal brief than a mere recitation of the claim elements and a naked assertion that the corresponding elements were not found in the prior art").

the first (130) and second (10) integrated circuit layers, wherein the first, second and third integrated circuit layers are stacked in a z-axis (vertical) direction (Fig. 4) and the third integrated circuit layer (120) comprises an interposer portion (below and to the left of the integrated circuit die (12) in Fig. 4) comprising an electrically conductive through via (40) configured to communicate with at least one interconnect element of the plurality of interconnect elements (24, 26, 28, 30, 32, 34, 58), and an integrated circuit die (12) adjacent to the interposer portion and between the first (130) and second (10) integrated circuit layers, wherein a surface of the integrated circuit die (12) comprises an electrical contact (14) electrically connected to the second integrated circuit layer (10) (by way of bonding wire 58, lead 30, via 50, via lead 26, via 40 and via pad 41a), and wherein the electrically conductive through via (40) of the interposer portion electrically connects the integrated circuit die (12) with the first integrated circuit layer (130) (col. 2, ll. 44–51, 58–63; col. 3, ll. 7–10, 14–18; col. 4, ll. 29–38; col.5, ll. 49–58; col. 5, l. 63 – col.6, l. 4; col. 6, ll. 21–23; Figs. 2–4).

The Appellants assert that Hayden does not meet the Appellants' claim 1's requirement that "the second integrated circuit is a semiconductor device that comprises the second plurality of interconnect elements" because 1) Hayden's integrated circuit chip (12) does not comprise a plurality of interconnect elements, and 2) Hayden's chip carrier (10) on which the integrated circuit chip (12) is mounted is a separate component from the integrated circuit chip (12) such that the integrated circuit chip (12) and the chip carrier (10) are not a single semiconductor device (App. Br. 8–9).

"'[D]uring examination proceedings, claims are given their broadest reasonable interpretation consistent with the specification.'" *In re*

Translogic Tech. Inc., 504 F.3d 1249, 1256 (Fed. Cir. 2007) (quoting *In re Hyatt*, 211 F.3d 1367, 1372 (Fed. Cir. 2000)). The Appellants do not point to written descriptive support in their Specification for claim 1's requirement that "the second integrated circuit is a semiconductor device". The Appellants' Specification indicates that the second integrated circuit layer (26C) can include non-semiconductor components and need not include a semiconductor component.[2] Thus, the Appellants' Specification indicates that the Appellants' claim term "semiconductor device" is at least as broad as that term's ordinary meaning, which is an "[e]lectronic device in which the characteristic distinguishing electronic conduction takes place within a semiconductor."[3] Thus, Hayden's integrated circuit layer 10, which includes an integrated circuit (12) (where the characteristic distinguishing electronic conduction within the layer takes place) and other components (e.g., chip carrier, bonding wire, traces and vias) is a semiconductor device according to the broadest reasonable interpretation of that term consistent with the Appellants' Specification.

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[2] "In some examples, passive elements configured to condition electrical signals within the stack may be positioned within IC layers 26A and 26C during fabrication. For example, IC layers 26A and 26C may be formed to include one or more passive resistors, inductors, capacitors, or any combination thereof" (¶ 33). "The semiconductor processing may be used to define the electrically conductive vias 32 and electrically conductive traces 34 in IC layers 26A and 26C within a semiconductor material (e.g., silicon). In addition, in examples in which IC layers 26C, 26C [sic, 26A, 26C] include semiconductor components, such as transistors in silicon, the components may be formed using the semiconductor processing techniques (e.g., as part of front-end-of-line (FEOL) processing)" (¶ 31).

[3] *McGraw-Hill Dictionary of Scientific and Technical Terms* 1790 (McGraw-Hill, 5th ed. 1994).

Claim 2

Claim 2 depends from claim 1 and requires that "the integrated circuit die does not include an electrically conductive through-via electrically connected to the first integrated circuit layer."

The Appellants assert that "Hayden fails to disclose that the figures illustrate a view of the IC chips 12, e.g., a cross-sectional view, that would even illustrate the detail of the IC chips required to establish that the IC chips does [sic] not include through-vias" (App. Br. 10) and that "the lack of mention of a particular feature, e.g., electrically conductive vias, by Hayden is not sufficient to establish that the system disclosed by Hayden does not include such a feature" (*id*).

Hayden discloses how the integrated circuit chip (12) is electrically connected to integrated circuit layer 130 (which corresponds to the Appellants' first integrated circuit layer), i.e., by way of bonding wire 58, lead 30, via 50, via lead 26, via 40 and via pad 41a (col. 3, ll. 7–10, 14–18; col. 4, ll. 29–38; Fig. 4). Hayden provides no indication that the electrical connection can be by way of an electrically conductive through via in that chip, either in addition to the disclosed electrical connection or as an alternative thereto. Consequently, there is sound reason for interpreting Hayden as disclosing that there is no through via in the integrated circuit chip (12) which electrically connects that chip to integrated circuit layer 130. *See In re Spada*, 911 F.2d 705, 708 (Fed. Cir. 1990) ("[W]hen the PTO shows sound basis for believing that the products of the applicant and the prior art are the same, the applicant has the burden of showing that they are not.").

Claim 4

Claim 4 depends from claim 1 and requires "a sensor layer coupled to an outer surface of at least one of the first integrated circuit layer or the second integrated circuit layer, wherein a characteristic of the sensor is configured to change in response to a tamper event."

Tucker discloses a secure chassis (102) comprising a container (106) having a base (105), sides (107) and a lid (104), each of which has a tamper sensor (112) for detecting unauthorized tamper events such as "removing access panels, drilling, or other means of gaining access to sensitive equipment or electronic components inside chassis **102**" (¶¶ 12, 15, 17). If the tamper sensor (112) detects an attempt to access a sensitive data-holding component such as a circuit card (124) located inside the chassis (102), a monitoring device (128) (not shown in the figures) can erase or encrypt the sensitive data or physically destroy the component (¶¶ 16, 18).

The Appellants assert that Tucker's tamper sensor (112) is between inner and outer portions of chassis walls, and that the Examiner has not shown that one of ordinary skill in the art looking to protect Hayden's chip layers would have had a reason with rational underpinning to couple Tucker's tamper sensor (112) to an outer surface of Hayden's chip layers (Reply Br. 9).

The Appellants appear to assert that their claim 4 requires the sensor layer to be positioned on the integrated circuit's outer layer. The coupling required by that claim, however, is electrical coupling, not physical coupling (Spec. ¶ 60). The Examiner finds that 1) Tucker's tamper sensor 112 is electrically coupled to circuit card 124 processing units through the monitoring device 128 to erase or encrypt the circuit card (124)'s sensitive

data or physically destroy the circuit card (124), 2) those processing units correspond to Hayden's integrated circuit layers, and 3) an electrical connection between Tucker's tamper sensor (112) and Hayden's input/output pads (137a, 139a, 141a, 156, 158, 160) which are electrically connected to Hayden's integrated circuit layers' outer surfaces and integrated circuit chips (12) would be required to erase data (Ans. 9). The Appellants do not indicate reversible error in those findings.

For the above reasons we are not persuaded of reversible error in the rejections as to claims 1, 2, 4–9 and 21–23.

Claims 11, 24 and 25

Claim 11 depends from claim 1 and requires that "the third integrated circuit layer further comprises a second integrated circuit die adjacent to the interposer portion".

The Examiner concludes that it would have been prima facie obvious to one of ordinary skill in the art to include a second die in Hayden's integrated circuit layer 120 to save space and because duplication of parts is obvious (Final Act. 5; Ans. 12).

Setting forth a prima facie case of obviousness requires establishing that the applied prior art would have provided one of ordinary skill in the art with an apparent reason to modify the prior art to arrive at the claimed invention. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). The Examiner does not establish that the relied-upon reason for adding a second die to Hayden's integrated circuit die 120 would have been apparent to one of ordinary skill in the art from Hayden's disclosure.

Claim 24 depends from claim 1 and requires "an integrated circuit package that houses the first, second, and third integrated circuit layers."

Hayden discloses that the individual chip layers (10, 120, 130, 132, 134) "are peripherally sealed to one another to form an hermetically sealed package" (Abstract; col. 10, l. 19).

The Examiner finds that Hayden's hermetically sealed package corresponds to the Appellants' integrated circuit package (Ans. 8).

The Examiner does not establish that Hayden's hermetic sealing of the individual chip layers to one another houses those layers as required by the Appellants' claim 24.

Claim 25 depends from claim 1 and requires that "the second integrated circuit layer further comprises a silicon substrate, and wherein the second plurality of interconnect elements are formed within the silicon substrate."

Wang discloses a through substrate via (TSV) flip chip comprising TSV contacts (1840) in a silicon substrate (col. 24, ll. 11–13; Fig. 20a).

The Examiner concludes that it would have been prima facie obvious to one of ordinary skill in the art to connect Wang's TSV flip chip to Hayden's device to increase its functionality (Ans. 15).

The Examiner does not establish that the Examiner's relied-upon reason for combining Hayden and Wang would have been apparent to one of ordinary skill in the art from their disclosures.

Thus, the Examiner has not established a prima facie case of anticipation of the system claimed in the Appellants' claim 24 or obviousness of the system claimed in the Appellants' claims 11 and 25.

DECISION/ORDER

The rejection of claims 1, 2, 9, 21, 22 and 24 under 35 U.S.C. § 102(b) over Hayden is affirmed as to claims 1, 2, 9, 21 and 22

and reversed as to claim 24. The rejections under 35 U.S.C. § 103 of claims 4–6 over Hayden in view of Tucker, claim 7 over Hayden in view of Heffner, claim 8 over Hayden in view of Michaels and claim 23 over Hayden in view of Lin are affirmed. The rejections under 35 U.S.C. § 103 of claim 11 over Hayden and claim 25 over Hayden in view of Wang are reversed.

It is ordered that the Examiner's decision is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED-IN-PART